Claims 1 and 3-5 (all the claims in this application) stand rejected under 35 USC §103(a) as being unpatentable over the U.S. Patent No. 6,088,783 to Morton in view of the U.S. Patent No. 4,670,518 to Potash. This rejection is respectfully traversed because, as will be explained below, it would not be obvious or even possible for a person skilled in the art to combine the teachings of Morton and Potash to arrive at the present invention.

Attached to this Response are illustrative Figures 1-4 which will be used in discussing the differences between the present invention and this newly cited prior art.

The key differences between the processor according to the invention and the one developed by Morton and Potash is the use of a core data transferring grid to transfer data from any Processor Element (PE) to any other PE. A Processor Element (PE) could be a register, ALU, memory, Cache, Input/Output port, video buffer, etc. There are endless examples of the use of data switches to transfer data to and from different devices but the concept of using them in a grid is unique to the present invention.

U.S. Patent No. 6,088,783 to Morton:

Morton does use a cross bar switch (109, P1) to transfer data from the data cache (108, P1) which is basically a switch that transfers data from Vector Processor (VP) to VP or from VP to data cache. To transfer data from the Vector Processor (110,111,112,113, P1) to the video buffer then would require data to pass through the data cache. The inventive system can transfer data directly from a vector processor or ALU to a video buffer. In addition, it can transfer data from the Vector Processor to the Video Buffer and from another Vector Processor to a memory interface in one cycle since there are multiple bus lines which can be defined by the programmer of the system.

Figure 1 (attached) shows a configuration of the inventive processor, set up to have the similar components as Morton, to show the difference in operation between the inventive system and the Morton system. The output of the ALU (100) can go directly to the memory interface via node switch (23) and the second ALU (200) can connect to the video buffer (101) via node switch (32). It is assumed that the ALU has an internal register to store the two data words to analyze.

The example shown in Figure 2 is the same as per Figure 1 except that the output of register B (102) is fed into the input of register A (202). This is a simple example which illustrates the difference between the inventive system and Morton. The inventive system can perform multiple tasks in the one clock cycle. The number of tasks per clock cycle depends upon the number required and also the size of the processor. Therefore, the more processor elements and node switches there are, the more functions that can occur in one cycle. Morton uses the cross bar switch to share data between parallel DSP chips and therefore to transfer data from one DSP chip to another DSP chip where the data must pass through the cross bar switch. Data cannot pass from the instruction unit (105) to Buffered, Video Aware, DMA Port (103) without passing though the instruction cache (104). This shows the key difference where the Morton processor needs to pass through other components to transfer data. Also there is only one data path for this operation, whereas the inventive system can have multiple data paths for the same operation. This allows the processor to have a failed unit, because data could still pass though another combination of data switches.

The inventive system is designed to be flexible in hardware design to allow the programmer to decide how to transfer data. If one wanted to transfer data from the output of ALU (100) to the Memory Interface (201) and also to the input of ALU (200) then nodes (23), and (21) could be switched to allow data to flow as per Figure 3.

With the system of the invention there are many switches in an array, rather than one component that allows data transfer such as the Cross bar switch (109, P1) of Morton with the inventive system, the instruction set is definable at the software level so that the way in which data is transferred is at the discretion of the programmer.

If a switch component such as node switch 23 fails, the system can still re-direct data through switches 22, 32 and 33 as shown in Figure 4 to allow data to transfer from the ALU (100) to the memory interface (201). The faulty switch can thus be bypassed to enable a functioning processor at the cost of a slightly less efficient system. Using this example of redundancy, if the ALU (100) failed then the ALU (200) could function in its place, and this would mean that instead of performing two ALU calculations at the one time, the two calculations would have to be done one after

another. The processor could know if there were a fault by checking the ALU with a set of calculation tests. A set of tests could also be executed for the switches and other processor elements.

This aspect of the invention has been mentioned merely to show the invention's potential and to illustrate how the invention differs from the prior art.

Concluding the discussion with respect to Morton's cross bar switch (109, P1), the key differences are that the inventive system does not rely upon one component to share data, and any Processor Element (PE) can connect to another Processor Element via a node switch. Data does not need to pass through a data cache or instruction cache. Also the inventive system can perform many PE to PE connections in one clock cycle, and the number of PE connections depends upon the size of the processor and thus the grid size.

Independent claim 1 of the present patent application defines components that are interconnected on a grid whereby a plurality of selected components can be switched under program control to a predetermined selection of other components. The inventive system can have components which connect directly to another component, via a connection of a

node as discussed in the application. The "predetermined selection" of interconnection can be made either by hardware or by software as described in the application specification. Morton's patent, as mentioned above, needs to pass data through a number of components to transfer data.

Finally, whereas Morton states in the abstract "*The parallel DSP chip executes a single task in parallel*" (Page 1, Abstract), the inventive processor can perform multiple instructions and provide multiple data paths.

Patent No. 4,760,518 to Potash:

The Potash patent states in the abstract that the bi-directional data-busing system "includes three sets of bi-direction memory data buses...". Consequently, Potash has a limited bus size whereas the inventive system can have a very large bus size depending upon the number of node switches. Potash also has a limited number of functional unit buses.

As can be seen in Figure 1 of Potash, in order to transfer data from the functional units *(e.g. two ALU's)* to the memory unit, the data must pass the Scalar XBAR which has a temporary memory for storing intermediate results.

Further, the present invention does not require such an intermediate stage. The Potash system has limited memory data buses, whereas the inventive system has a much higher number of memory data buses, with the number of memory buses being defined by the processor size. Looking at Figure 1 to Potash again it can be seen that there are a limited number of functional unit buses as well. Since there are limited buses, this makes the inventive system, which is expandable at will, very different. Potash relies on vector registers (36-38, Fig. 1) and scalar registers (42, Fig. 1) to store data in order to be able to later process it. The inventive system can transfer data directly from memory to an ALU and, if the ALU processes the result in the same clock cycle, it can then output this result, all in the one clock cycle as shown in Figure 4 of this application.

It will be appreciated, from this limited explanation of both Morton and Potash, that it would not be a simple matter to combine the teaching of both these patents to arrive at the present invention. Added to this is the simple fact that there is no suggestion, either in Morton or Potash, to make a combination of such divers prior art systems.

Accordingly, while on their face, Morton and Potash teach the general subject matter of the present invention, on closer scrutiny, these patents do not teach the use of a grid with a plurality of node switches to interconnect the components of a computer system.

Accordingly, independent claim 1 and dependent claims 3-5 are believed to distinguish patentably over the prior art of record. The immediate allowance of claims 1 and 3-5 is respectfully solicited.

Respectfully submitted,

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AUGUST 9, 2004

MILDE & HOFFBERG, LLP

By _____

Date AUGUST 9, 2004